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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,742	09/10/2003	Martin Brox	006410.00001	3389

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EXAMINER	
LUU, AN T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,742	BROX, MARTIN	
	Examiner	Art Unit	
	An T. Luu	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 September 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2-3-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-11 and 13-19 are rejected under 35 U.S.C. 102(b) as being anticipated by the Frisch et al reference (U.S. Patent 5,644,261).

Frisch discloses in figure 6 an apparatus for converting a signal (input of 76) into a corresponding delayed signal (output of bottom inverter), comprising a plurality of signal delay elements (delay elements 76) connected in series, wherein, as a function of the desired delay of the delayed signal (output of bottom inverter), the respective output signal of a particular signal

delay element (via switches 34) is used for generating the delayed signal, wherein said signal delay elements each comprise one single inverter only as required by claim 1.

As to claim 2, figure 6 shows the apparatus outputs the respectively desired delay from the respective signal delay element used for generating the delayed signal which is inverted or non-inverted vis-à-vis the signal (input of 76).

As to claim 13, the apparatus shown in figure 6 has at least three signal delay elements connected in series.

As to claim 14, figure 6 shows the signal delay elements 76 are respectively connected with corresponding gates 34; wherein as a function of the respectively desired delay - that gate is activated that is connected to the signal delay element whose output signal is to be used for generating the delayed signal; and wherein, depending on whether the output signal of a particular signal delay element is inverted or non-inverted vis-à-vis the signal, the gate connected with the respective signal delay element is designed such that it advances the output signal in non-inverted or in inverted manner.

As to claim 15, figure 6 shows the output signal of a particular signal delay element (first left inverter 76) being inverted vis-à-vis the signal, the gate connected with the respective signal delay element is designed such that it advances the output signal in an inverted manner (i.e., the output of the leftmost inverter 76 has to pass through additional two inverters) and, when the output signal of a particular signal delay element is non-inverted vis-à-vis the signal (signal outputted from the second inverter 76), the gate connected with the respective signal delay element is designed such that it advances the output signal in a non-inverted manner (i.e., the output of the leftmost inverter 76 has to pass through additional two inverters) and, when the

output signal of a particular signal delay element is non-inverted vis-à-vis the signal (signal outputted from the second inverter 76).

As to claims 16-19, figure 6 shows an inverter coupled between the delay element and the gate for providing a function as required by the claim (i.e., the output signal of a particular signal delay element is inverted vis-à-vis the signal, the gates connected with the respective signal delay element is designed such that it advances the output signal in a non-inverted manner and, when the output signal of a particular signal delay element is non-inverted vis-à-vis the signal (IN), the gate connected with the respective signal delay element is designed such that it advances the output signal in an inverted manner).

As to claim 3, the apparatus shown in figure 6 has at least three signal delay elements connected in series.

As to claims 4 and 5, figure 6 shows the signal delay elements are respectively connected with corresponding gates 34, wherein as a function of the respectively desired delay - that gate is activated that is connected to the signal delay element whose output signal is to be used for generating the delayed signal.

As to claim 6, figure 6 shows depending on whether the output signal of a particular signal delay element is inverted or non-inverted vis-à-vis the signal, the gate connected with the respective signal delay element is designed such that it advances the output signal in non-inverted or in inverted manner.

As to claim 7, figure 6 shows the output signal of a particular signal delay element (first left inverter 76) being inverted vis-à-vis the signal, the gate connected with the respective signal delay element is designed such that it advances the output signal in an inverted manner (i.e., the

output of the leftmost inverter 76 has to pass through additional two inverters) and, when the output signal of a particular signal delay element is non-inverted vis-à-vis the signal (signal outputted from the second inverter 76), the gate connected with the respective signal delay element is designed such that it advances the output signal in a non-inverted manner (i.e., the output of the leftmost inverter 76 has to pass through additional two inverters) and, when the output signal of a particular signal delay element is non-inverted vis-à-vis the signal (signal outputted from the second inverter 76).

As to claim 8, the scope of claim 7 is similar to that of claim 7. Therefore, it is rejected for the same reason set forth above. It is noted that the output signal of the apparatus is seen as taken at the output of the transfer gate 34.

As to claim 9, it is anticipated by transfer gate 34 or an inverter coupled between inverter 76 and transfer gate 34.

As to claims 10 and 11, figure 6 discloses two inverters and a transfer gate being configured as recited in claims (i.e., two unlabeled inverter and transfer gate 34 in series connection between output of inverter 76 and the output of the apparatus).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 12 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Frisch et al reference (U.S. Patent 5,644,261) in view of the Nii reference (U.S. Patent 6,624,667).

Frisch discloses all the claimed invention except for teaching the use of tri-state inverter as required by claim 12.

Nii discloses in figure 3 a tri-state inverter 8 within a series connected inverters as required by the claim.

It would have been obvious to one skilled in the art at the time the invention was made to replace an inverter of Frisch with a tri-state inverter taught by Nii since an inverter is known to come in different type, size or shape.

A skilled artisan in the art would have been motivated to combine the above arts since a tri-state inverter provides a reduced current consumption and lower noise, and enhanced insensitivity to the in-phase noise.

As to claim 20, the scope of claim is similar to that of claim 12. Therefore, it is rejected for the same reason set forth above.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to An T. Luu whose telephone number is 571-272-1746. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

An T. Luu
9-30-04 ATL

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